IN THE CLAIMS

The pending claims are reproduced herein for the Examiner's convenience:

1. (Previously Presented) A process of forming a metallization comprising:

forming a first interlayer dielectric (ILD) layer above a substrate;

forming a first recess in the first ILD layer;

filling the first recess with a first interconnect;

forming a conductive first diffusion barrier layer above and on the first interconnect;

forming an upper ILD layer above the first conductive diffusion barrier layer;

forming an upper recess in the upper ILD layer to optionally expose the first conductive diffusion barrier layer;

forming an upper interconnect in the upper recess; and

forming a conductive upper diffusion barrier layer above and on the upper interconnect.

2. (Previously Presented) A process of forming a metallization comprising:

forming a first interlayer dielectric (ILD) layer above a substrate;

forming a first recess in the first ILD layer;

filling the first recess with a first interconnect;

forming a conductive first diffusion barrier layer above and on the first interconnect;

forming an upper ILD layer above the first conductive diffusion barrier layer;

forming an upper recess in the upper ILD layer to expose the first conductive diffusion barrier layer;

forming an upper interconnect in the upper recess; and

forming a conductive upper diffusion barrier layer above and on the upper interconnect, wherein at least one of forming a conductive first diffusion barrier layer and forming a conductive upper diffusion barrier layer includes:

electroless plating the conductive diffusion barrier layer.

3. (Original) The process according to claim 1, wherein at least one of forming a conductive first diffusion barrier layer and forming a conductive upper diffusion barrier layer includes:

vapor depositing the conductive diffusion barrier layer, selected from chemical vapor deposition, plasma-enhanced chemical vapor deposition, atomic layer chemical vapor deposition, and physical vapor deposition.

4. (Original) The process according to claim 1, further including:

forming a barrier film in at least one of the first recess and the upper recess; and

optionally forming a conductive seed film over the barrier film.

5. (Previously Presented) The process according to claim 1, further including:

forming a barrier film in at least one of the first recess and the upper recess;

forming a conductive diffusion barrier film over at least one of the barrier films; and

optionally forming a conductive seed film over the conductive diffusion barrier film.

6. (Original) The process according to claim 1, wherein forming a first ILD layer includes forming an organic ILD layer, further including:

forming a hard mask above and on the organic ILD layer; and

patterning an opening in the hard mask.

7. (Original) The process according to claim 1, further including:

forming a first hard mask above and on the first ILD layer;

patterning an opening in the first hard mask;

forming an upper hard mask above and on the upper ILD layer;

patterning an opening in the upper hard mask.

8. (Original) The process according to claim 1, wherein forming a first ILD layer includes:

forming an inorganic first bottom ILD layer; and

forming an organic first top ILD layer.

9. (Original) The process according to claim 8, wherein forming a first recess includes:

forming a dual-damascene recess in the inorganic first bottom ILD layer and in the organic first top ILD layer.

10. (Original) The process according to claim 9, further including:

forming a first hard mask above and on the organic first top ILD layer; and

patterning an opening in the first hard mask.

11. (Previously Presented) A process of forming a metallization comprising:

forming a first interlayer dielectric (ILD) layer above a substrate;

forming a first recess in the first ILD layer;

filling the first recess with a first interconnect;

forming a conductive first diffusion barrier layer above and [[an]] on the first interconnect;

forming an upper ILD layer above the first conductive diffusion barrier layer;

forming an upper recess in the upper ILD layer to optionally expose the first conductive diffusion barrier layer;

forming an upper interconnect in the upper recess; and

forming a conductive upper diffusion barrier layer above and on the upper interconnect, wherein forming an upper ILD layer includes:

forming an inorganic upper bottom ILD layer; and

forming an organic upper top ILD layer, and wherein forming an upper recess includes forming a dual-damascene recess in the inorganic upper bottom ILD layer and in the organic upper top ILD layer, wherein forming a first ILD layer includes:

forming an inorganic first bottom ILD layer; and

forming an organic first top ILD layer.

12. (Original) The process according to claim 11, further including:

forming an upper hard mask above and on the upper bottom ILD layer; and

patterning an opening in the upper hard mask.

13. (Original) The process according to claim 1, wherein forming a first ILD layer includes:

forming an organic first bottom ILD layer; and

forming an inorganic first top ILD layer.

14. (Original) The process according to claim 13, wherein forming a first recess includes:

forming a dual-damascene recess in the organic first bottom ILD layer and in the inorganic first top ILD layer.

15. (Original) The process according to claim 14, further including:

forming a first hard mask above and on the organic first bottom ILD layer; and

patterning an opening in the first hard mask.

16. (Original) The process according to claim 13, wherein forming an upper ILD layer includes:

forming an organic upper bottom ILD layer; and

forming an inorganic upper top ILD layer, and wherein forming an upper recess includes forming a dual -damascene recess in the organic upper bottom ILD layer and in the inorganic upper top ILD layer.

17. (Original) The process according to claim 16, further including:

forming an upper hard mask above and on the upper bottom ILD layer; and patterning an opening in the upper hard mask.